Neo900 Hackerbus

PRELIMINARY – SUBJECT TO CHANGE WITHOUT FURTHER NOTICE

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The Hackerbus is an interface that allows user-provided circuits to connect directly to power rails and various signals in the Neo900.

Warning: Hackerbus gives access to signals that can upset the operation of the Neo900 and incorrect use may cause permanent damage inside and outside the device. Use with caution !

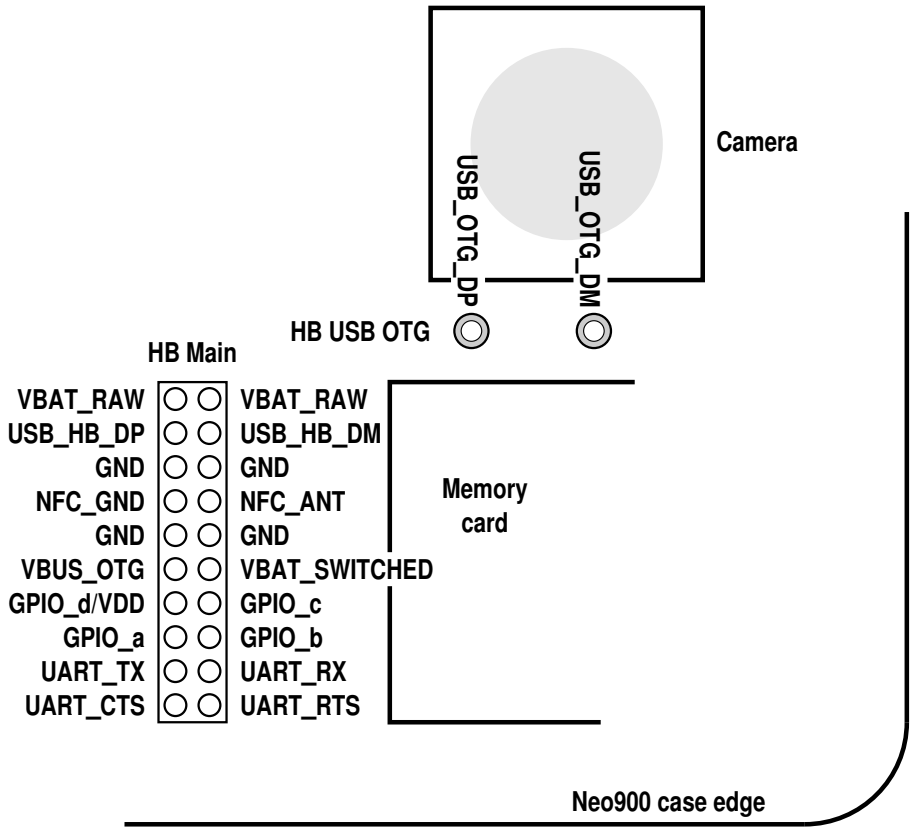
Characteristics beyond what is specified in this document should be obtained by examining the schematics and the data sheets of the respective components.

*Concept and design requirements.
†Specification details and illustrations.

1 Pin assignment

Hackerbus uses two connectors, one for power and various signals and one for USB OTG data, which are arranged around the memory card on the Break-Out-Board (BOB).

The following drawing gives a rough overview of connector locations and shows the pin assignment:



The following table describes the functions of the pins on the Hackerbus main connector:

Hackerbus pin	**Description**
VBAT_RAW	Direct connection to the battery (charging allowed)
VBAT_SWITCHED	Like VBAT_RAW but switched off when system is powered down **Reverse-feed not allowed !**
VBUS_OTG	USB OTG bus voltage (reverse-feed allowed)
GND	System ground and return for power and all signals but NFC and audio
USB_HB_DP	USB differential data, positive
USB_HB_DM	USB differential data, negative
UART_TX	UART3, Transmit data (output from CPU)
UART_RX	UART3, Receive data (input to CPU)
UART_CTS	UART3, Clear To Send (input to CPU)
UART_RTS	UART3, Ready To Send (output from CPU)
GPIO_a	TBD
GPIO_b	TBD
GPIO_c	TBD
GPIO_d/VDD	TBD / VAUX3 rail
NFC_ANT	NFC antenna, positive
NFC_GND	NFC antenna, ground or negative **Do not connect to any other GND !**

Note that the UART signals may also be used as general IOs and that their role further depends on the configuration of the infrared (IR) subsystem [1].

TO DO: The exact function of UART_RX will depend on the implementation of IR RX, which will be decided at a later time.

The Hackerbus USB OTG through-hole pads give access to signals from the Neo900 Micro USB connector:

Hackerbus pin	**Description**
USB_OTG_DP	USB differential data, positive
USB_OTG_DN	USB differential data, negative

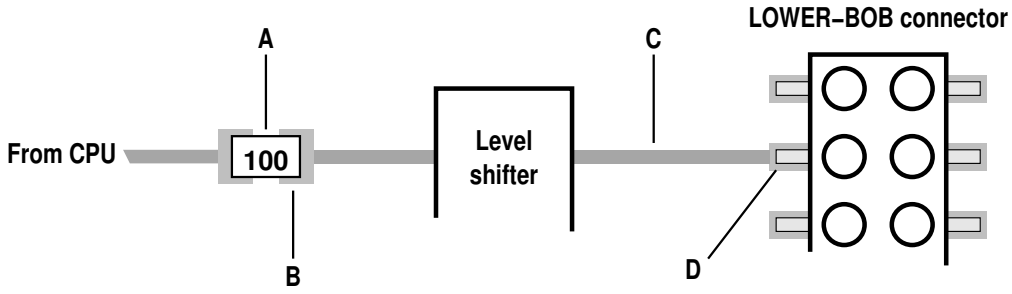
Further details on how Hackerbus connects to USB can be found in section 3.

2 Alternate pin assignments

Some Hackerbus pins are prepared for modifications that allow alternative signals to be assigned to them. The following list shows the pins that can be reassigned:

Group	Signal
UART	HB_TX_IRTX
	HB_CTS_RCTX
	UART3_RTS
	UART3_RX_IRRX
GPIO	HB_A
	HB_B
	HB_C
	HB_D

The circuit of these signals is located on the LOWER PCB and looks as follows:



The resistor **A** can be removed to separate the signal from the CPU. The alternative signal can be attached with a jumper wire either at point **B** (if digital) or point **D** (if analog). The trace can be cut between level shifter and LOWER-BOB connector (**C**) to separate the pin also from the level shifter (see section 6), but we know of no technical need for doing this. The following alternative signals are available on a patch field near the LOWER-BOB connector:

Group	Signal	Type
I^2C	I2C3_SDA	Digital
	I2C3_SCL	Digital
USB	OTG_ID	Analog
Audio line in/out	HB_LINE_OUT_L	Analog
	HB_LINE_OUT_R	Analog
	HB_LINE_IN	Analog
Audio jack	HB_JACK_1L	Analog
	HB_JACK_2R	Analog
	HB_JACK_3M	Analog
	HB_JACK_4GND	Analog
Digital microphone	HB_DMIC_CLOCK	Digital
	HB_DMIC_DATA	Digital

To choose an alternative assignment, the circuit of the respective pin has to be modified as follows:

Digital signal
: If the original signal is shared with other functions (e.g., UART), remove the resistor at **A**. Then connect the new signal with a jumper wire between the patch field and point **B**.

Positive analog signal
: If the original signal is shared with other functions (e.g., UART), remove the resistor at **A**. Solder the jumper wire with the new signal to the respective pin on the LOWER-BOB connector (**D**).

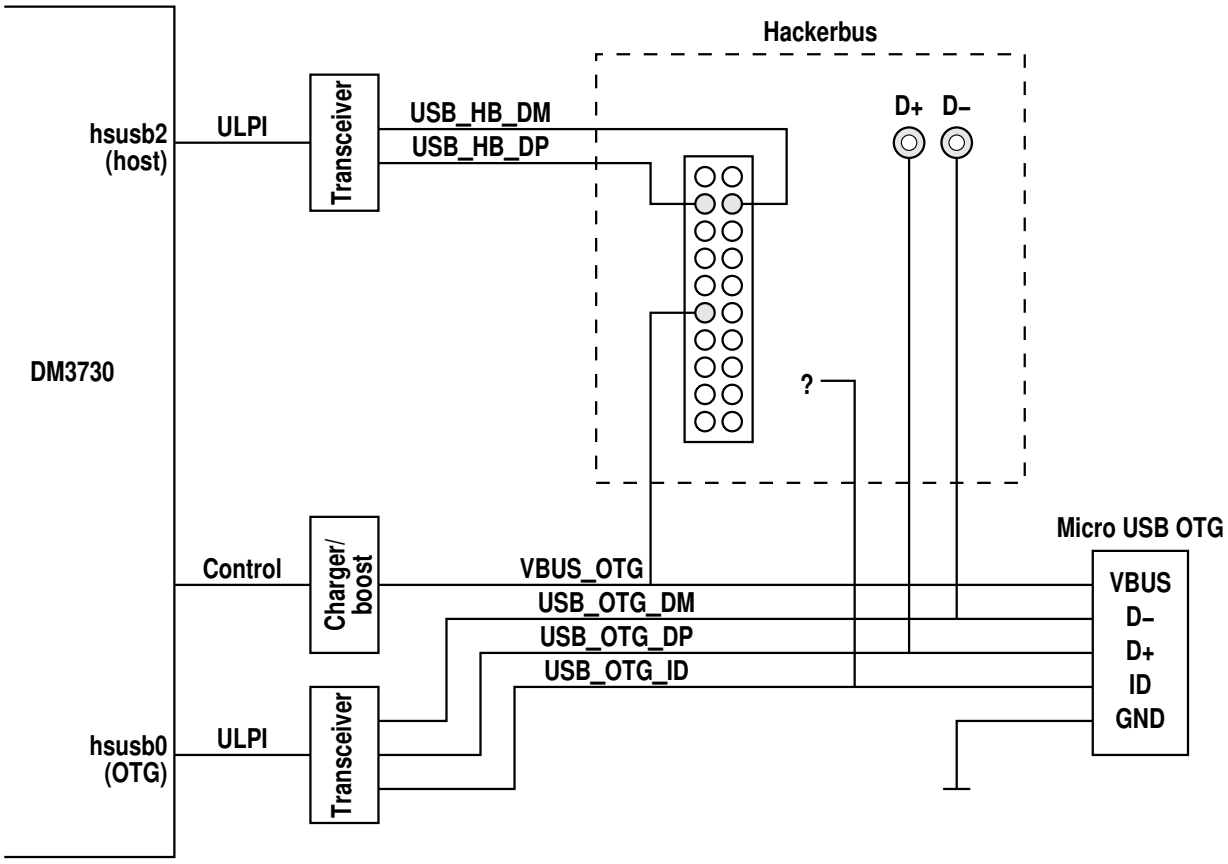
Negative analog signal
: If the analog signal can become negative (with respect to ground), conflict with the clamp diode in the CPU may occur. Therefore, remove the resistor at **A** and solder the jumper wire to **D**. Note that the ESD protection may also interfere with the signal.

Note that, if the resistor is not removed, the CPU typically has to tri-state the respective signal.

3 USB access

Hackerbus gives access to two USB buses: the data signals of a High-Speed host port are available on the Hackerbus connector. This USB port is used exclusively for Hackerbus.

Furthermore, the data signals of the Neo900 USB OTG port (High-Speed) are available on contacts accessible from the Hackerbus, VBUS of the OTG port is available on the Hackerbus connector, and the ID signal of OTG is available as an alternate pin assignment. (See section 2.)

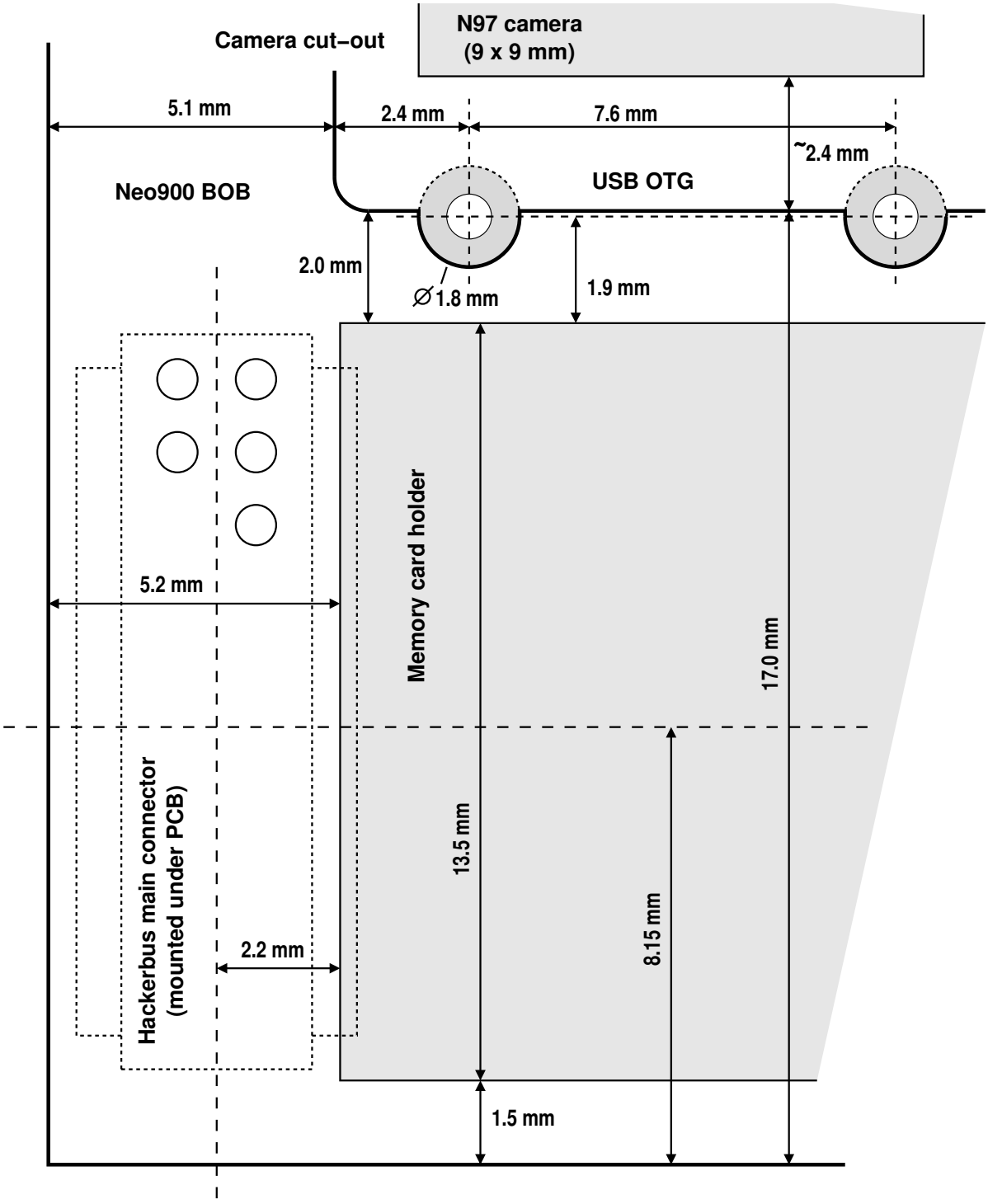


TO DO: Define and indicate alternate pin assignment for USB ID.

Note that there is no bus supply voltage (VBUS) on the dedicated USB interface of Hackerbus. User circuits can be powered from the 2.7 V rail or from any of the other supplies.

4 Physical placement

The following drawing illustrates the precise placement of components on the Break-Out-Board (BOB):



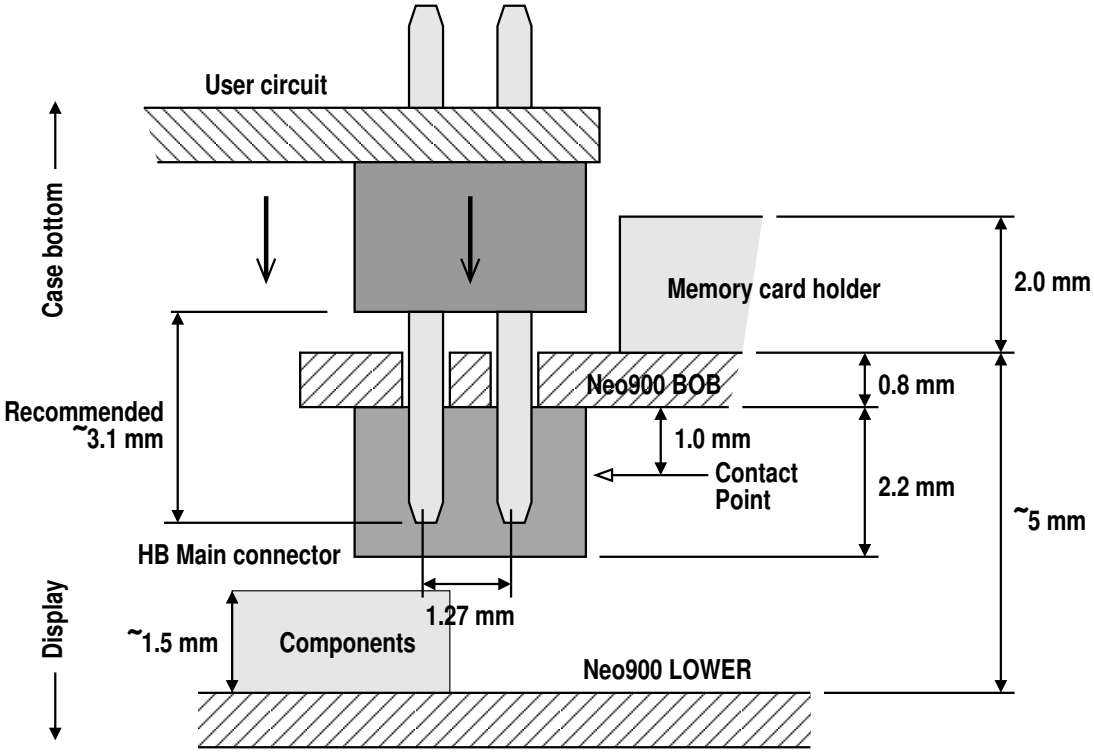
The main connector is soldered to the bottom of the BOB and the header pins pass through holes in the PCB, entering the receptacle from the bottom. The USB OTG contacts are on the LOWER board of Neo900 and can be accessed through an opening in the BOB.

Please note that the Hackerbus connector and contacts are covered by plastic structures in the N900 case and are therefore only accessible when the case is removed or if the respective plastic structures have been cut.

4.1 Hackerbus main connector

On the Neo900 side, the principal connector for Hackerbus is a Harwin M50-3151042 [2] female connector with 20 contacts organized in a 10×2 array. The connector has a 1.27 mm pitch and is mounted underneath the Neo900 break-out board (BOB).

The vertical stacking of the main connector is illustrated in the following diagram:[1]



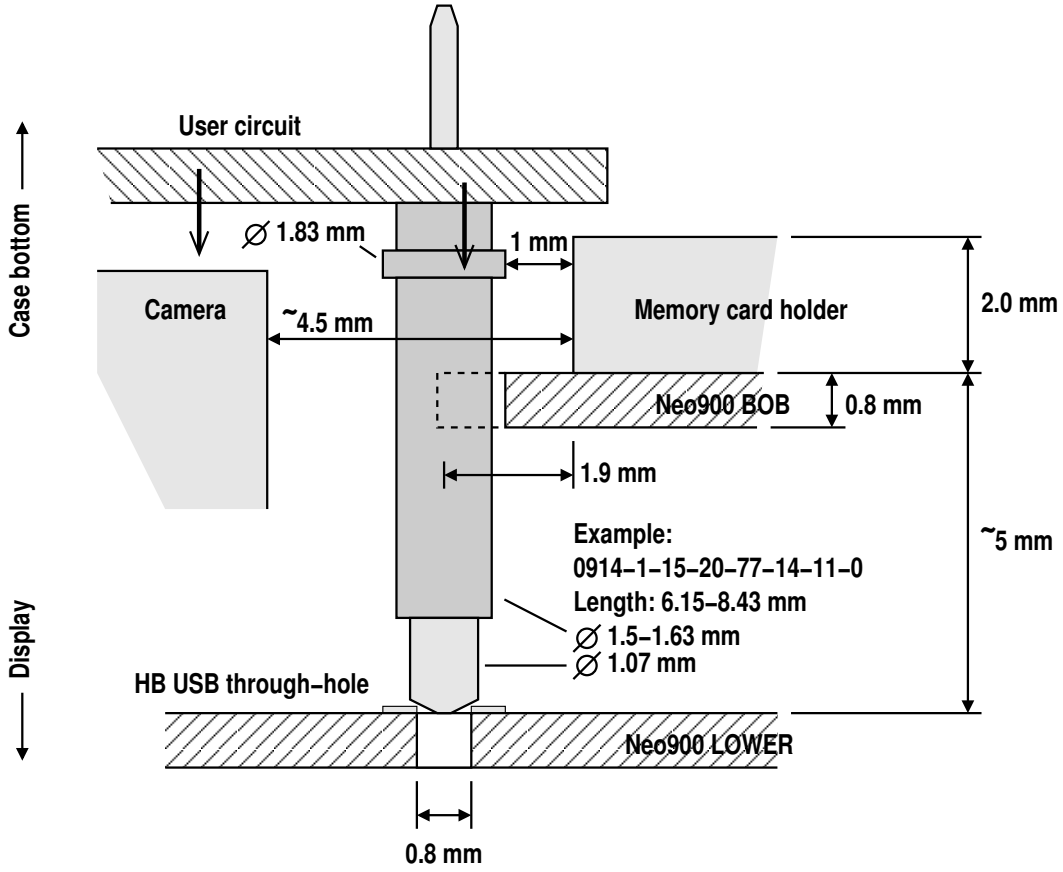
The male header shown as an example in the drawing has the dimensions of the FCI 20021111-00020T4LF through-hole connector,[2] with a contact length of 3.05 mm and a plastic mold height of 2.5 mm. (See also [3].)

[1] The drawing is approximately to scale but dimensions drawn can be off by up to 0.15 mm in real-world coordinates.
[2] `http://portal.fciconnect.com/Comergent/fci/drawing/20021111.pdf`

4.2 Hackerbus USB OTG contacts

On the Neo900 side, the USB OTG contacts for Hackerbus consist of two through-hole pads in the LOWER board. Cut-outs in the BOB allow them to be accessed with pogo pins on the user board.

The vertical stacking of the USB OTG connection is illustrated in the following diagram:

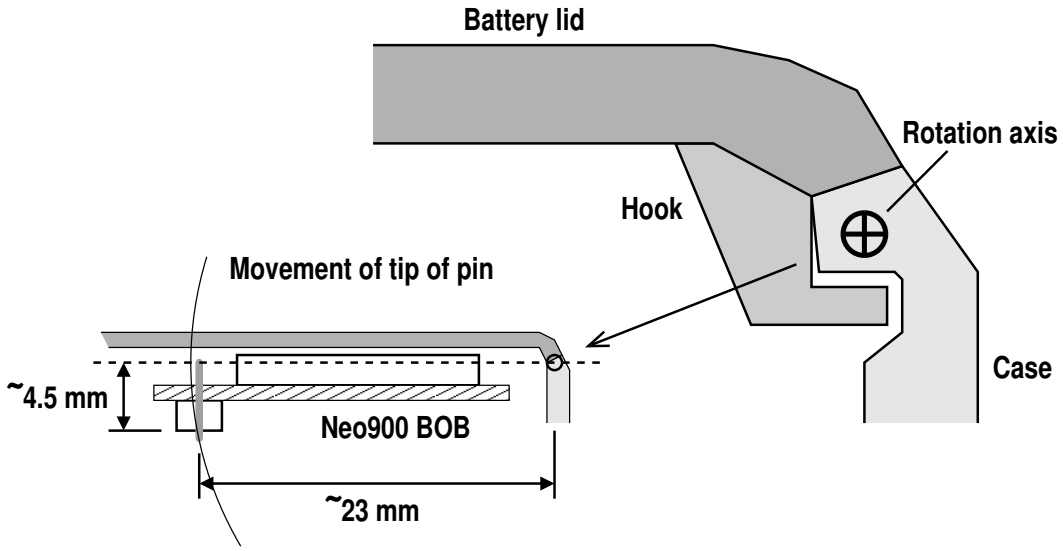


The characteristics of the pogo pins depend on the placement of the user board. Clearances and hole diameters are designed for the Mill-Max 914 series. [4] The following table shows minimum, middle, and maximum length of the pogo pins in this series. The length corresponds to the distance between the facing sides of LOWER and the user board.

Part number	Length (mm)		
	Min.	Mid	Max.
0914-**0**-15-20-77-14-11-0	5.38	6.53	7.67
0914-**1**-15-20-77-14-11-0	6.15	7.29	8.43
0914-**2**-15-20-77-14-11-0	6.91	8.05	9.19
0914-**3**-15-20-77-14-11-0	7.67	8.82	9.96

4.3 Mechanical coupling with battery cover

If the user circuit connecting to Hackerbus is mechanically coupled with the battery cover, the movement when opening and closing the battery compartment has to be considered. The following drawing shows approximately how the parts involved move:



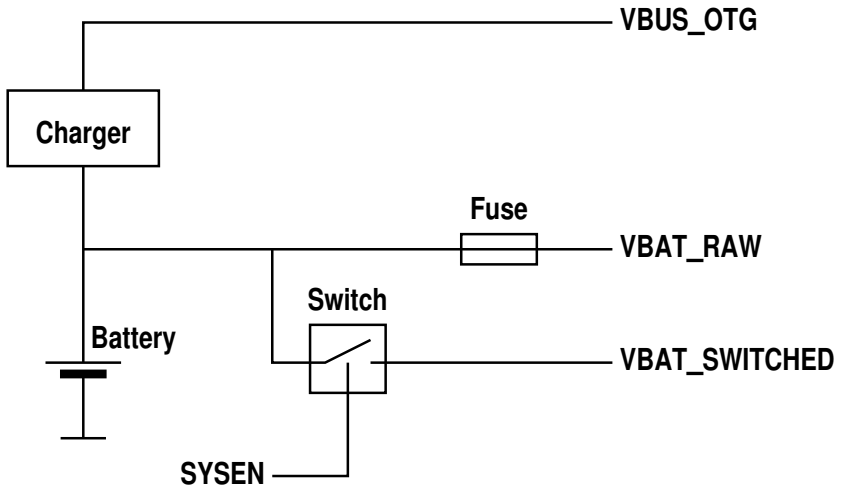
The cover has a hook that goes into an opening in the case. When opening or closing the cover it rotates around that hook, which results in anything mechanically connected to the cover to perform the same rotation.

The drawing shows the path along which a header pin plugging into the Hackerbus main connector moves. This rotation may make it difficult to connect extensions whose Hackerbus connector is rigidly coupled with the battery cover. These difficulties would be more pronounced for the Hackerbus USB connector since it is closer to the axis around which the battery cover rotates.

Possible ways to avoid this issue include not coupling the extension with the battery lid, using a flexible coupling, or removing the hook on the cover.

5 Overcurrent protection

To protect traces and other components from excessive current, VBAT_RAW is equipped with a resettable fuse. Traces and contacts between battery and Hackerbus are designed to be able to permanently conduct at least the trip current of the fuse.



Note that the presence of this fuse does not guarantee that loads exceeding the trip current will not lead to malfunction. Furthermore, the battery is a user-provided item and needs to be evaluated separately by prospective users of VBAT_RAW. The maximum current available on VBAT_RAW depends not only on the fuse but also on the characteristics and condition of the battery.

The design of Neo900 is intended to support the following maximum currents without suffering damage or disturbing normal system operation, provided that suitable power sources are available:

Hackerbus pin	Continuous current (A)	
	Forward	Reverse
VBAT_RAW	0.5	1.5
VBAT_SWITCHED	0.3	—
VBUS_OTG	0.5	0.5
GPIO_d/VDD	0.2	—

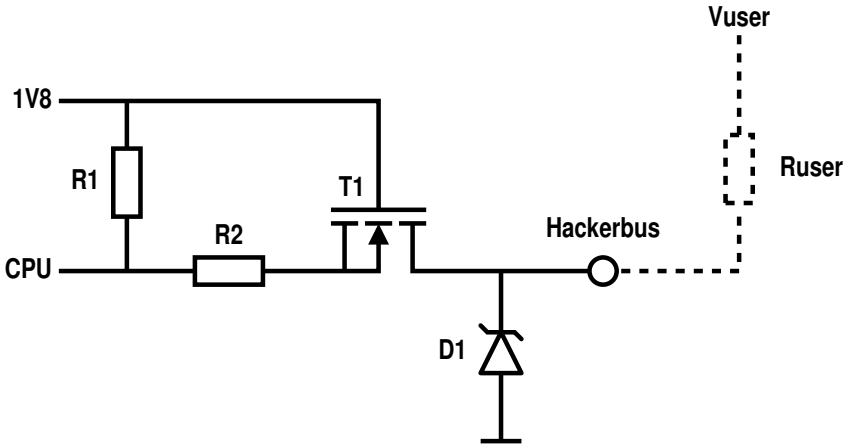
All these limits apply to individual rails. Predicting behaviour when drawing or injecting significant current on multiple rails at the same time is beyond the scope of this document.

Please note that none of these parameters are guaranteed, and further constraints may apply.

Peripherals using VBAT_RAW should connect to both VBAT_RAW contacts with traces that each are capable of carrying the full maximum current the application demands.

6 Level shifters

Level shifters are provided to interface with circuits operating in other domains than 1.8 V. The circuit is as follows, for each primary UART and GPIO signal:



The principle of operation is briefly described in [5] and further details can be found in [6]. R1 is usually an internal pull-up resistor in the CPU of 10 kΩ or higher. R2 limits the current when CPU and external circuit drive the Hackerbus signal in a conflicting way. R2 is 100 Ω. D1 protects against ESD and polarity inversion.

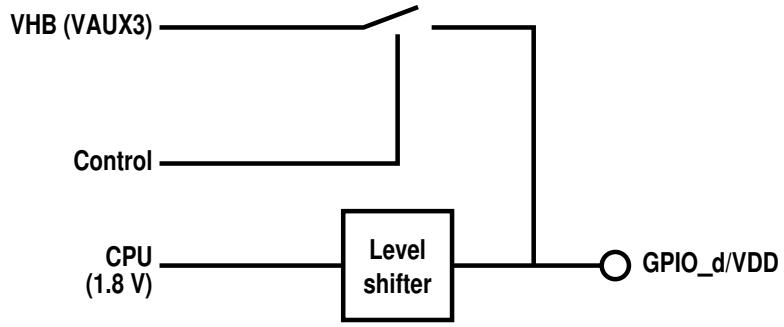
Note that our circuit differs from the NXP design in that Neo900 does not provide a pull-up resistor on the high-voltage side. If the user circuit needs a pull-up, e.g., to drive a logic input, it therefore has to provide one itself. If an external pull-up is to be used, it should be dimensioned such that it does not deliver more than 1.8 mA into the Neo900 if the corresponding Hackerbus signal is driven low (0 V). A value of 10 kΩ or larger is recommended.

Power, NFC, USB, and secondary signals (other than I2C) are not equipped with level shifters.

Further limits and characteristics of this circuit are to be determined by the user.

7 Switchable power rail

The VHB power rail (corresponding to the VAUX3 regulator) can be switched to the GPIO_d pin under software control. If not operating as power rail, GPIO_d can be used for regular IO. The following drawing illustrates the circuit:



VAUX3 provides up to 200 mA. The voltage can be set by software to 1.5, 1.8, 2.5, 2.8, or 3.0 V.

The connection to the CPU is protected by the same circuit as all other IOs available on the Hackerbus. When GPIO_d is configured as power rail, the CPU should set the corresponding GPIO to High-Z without pull-up or -down. The CPU may read the GPIO, but the resulting value is undefined.

A LOWER-BOB connection

The design of Hackerbus also affects the connection between LOWER and BOB. We therefore discuss characteristics of the connection in this appendix, and provide a design that harmonizes with Hackerbus.

A.1 Signals

In addition to the 20 signals of the Hackerbus main connector described in section 1, we have the following signals to other components on BOB:

Signal(s)	Number	Connects to ...	Maximum average current
SD-CMD,CLK,DATx	6	Memory card holder	
SD-VDD	1	Memory card holder	100 mA (?)
SD-CD	1	Memory card holder	
I2C-SDA,SCL	2	Flash, camera cover sensor	
CAM-COVER	1	Camera cover sensor	
BATT-LID	1	Battery lid sensor	
2V7	1	Camera and battery sensor	50 mA[3]
PRIVACY-R,G,B	3	Privacy LED	
FLASH-A,K	2	Flash LEDs	300 mA[4]
GND	1	All of the above	Sum of the above, 450 mA
	19		

We expect that each contact of the board-to-board connector can support a maximum continuous current of 0.5 A (section A.3). None of the above signals exceeds this limit.

This brings the total number of contacts required to 39: 20 for Hackerbus plus another 19 for the remaining functions of BOB.

A.2 Connector characteristics

The most important parameter is the distance between boards. Measurements based on 3D scans of a N900[5] yielded an approximate distance of 5.2-5.3 mm between the bottom (i.e., the battery-facing side) of LOWER and the bottom of BOB. Given a PCB thickness of 0.8 mm, this means that we need connectors with a stacking height of approximately 4.4-4.5 mm.

To ensure precise placement of the connectors, positioning pins ("board guides") are desirable.

[3] The MLX90248 hall switch for camera cover sensing has a maximum current consumption of 5 mA. The TMD2671 proximity sensor used on the battery lid has a supply current of 3 mA plus LED pulses of up to 100 mA with a duty cycle of $^{7.2\ \mu s}/_{16.3\ \mu s} = 44\%$.

[4] Absolute maximum peak pulsed LED forward current in table 4 of `http://www.lumileds.com/uploads/461/DS209-pdf`

[5] `https://neo900.org/git/scans/plain/data/stl/n900-rear-open-nobat-100um.stl.bz2`

A.3 Connector selection

A Digi-Key catalog search yielded the following connector families with good availability of parts:

Series	Stacked height (mm)	Pitch (mm)	Current per pin (A)	Cycles (max.)
FCI Conan[6]	4.5	1.0	1.0	30
Hirose DF9[7]	4.3	1.0	0.5	30/100[8]
Harwin M40[9]	4.3	1.0	0.5	30

All three have a contacts in a trapezoidal arrangement with N contacts in one row and $N + 1$ in the other, and very similar footprints. Positioning pins and solder retention are optional in some series:

Series	Positioning pin length (mm)	Solder retention
FCI Conan	0.5 mm, optional	yes
Hirose DF9	1.0 mm, optional	optional
Harwin M40	1.0 mm	yes

Hirose DF9 and Harwin M40 appear to have exactly the same geometry. FCI Conan has nearly the same contact arrangement, but the positioning pins are placed differently and the overall length is reduced. Note that the length of the positioning pins of DB9 and M40 exceeds the PCB thickness.

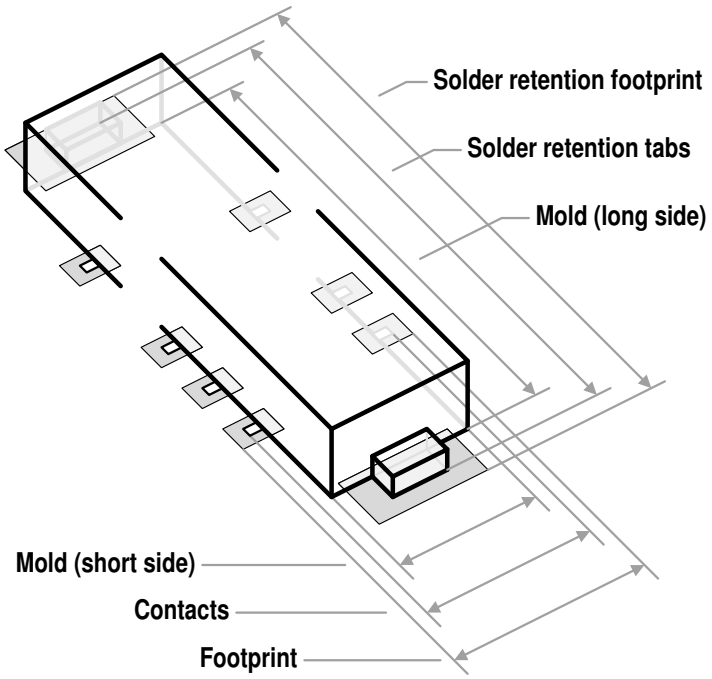
The stacking height of DF9/M40 (4.3 mm) matches the desired height of 4.5 mm within measurement and manufacturing tolerances. Conan matches the height exactly.

We will only consider connectors with at least 15 contacts and a footprint not exceeding the available PCB width of 17 mm.

A.4 Connector dimensions

The following tables list the dimensions of the "bounding boxes" of the bodies and the footprints of the three connector families selected in the previous section. This stylized drawing illustrates the parameters we consider:

[6] `http://portal.fciconnect.com/Comergent//fci/drawing/91900.pdf`
[7] `http://media.digikey.com/pdf/Data%20Sheets/Hirose%20PDFs/DF9.pdf`
[8] Tin vs. gold plating.
[9] `http://cdn.harwin.com/pdfs/M40-600.pdf`
`http://cdn.harwin.com/pdfs/M40-620.pdf`



For the long sides we have the length of the body, and the edge-to-edge distance of metal tab and footprint of the solder retention. The body length is either the length of the plastic mold (in the case of Conan, where the mold protrudes) or the distance between the ends of the solder retention tabs (DF9/M40, where the tabs protrude), whichever is larger.

Series	Contacts	Body (mm) Solder retention with	Body (mm) Solder retention without	Solder retention footprint (mm)
FCI Conan	15	12.30	—	11.84
	21	15.30	—	14.84
	25	17.30	—	16.84
Hirose DF9	15	13.1	11.3	14.0
	17	14.1	12.3	15.0
	19	15.1	13.3	16.0
	21	16.1	14.3	17.0
Harwin M40	15	13.10	—	14.00
	21	16.10	—	17.00

Only configurations with solder retention tabs and with 15 and 21 pins are available from more than one source.

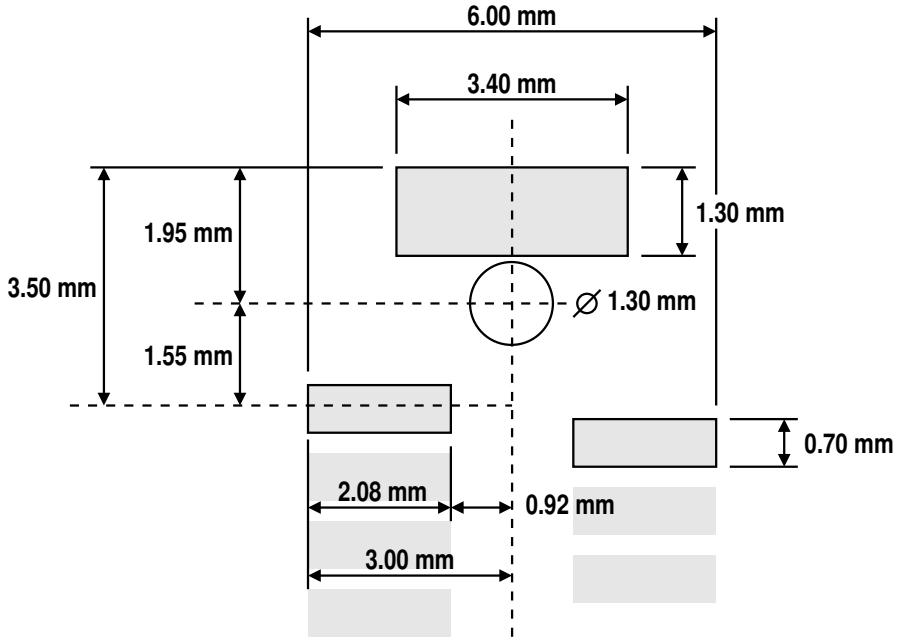
For the short sides, we consider the width of the mold, the length of the protruding contacts (if any), and the edge-to-edge distance across the PCB pads for the contacts.

Series	Mold (mm)	Contacts (mm)	Footprint (mm)
FCI Conan	5.59	—	5.85
Hirose DF9	4.2	5.6	6.0
Harwin M40	4.20	5.60	6.00

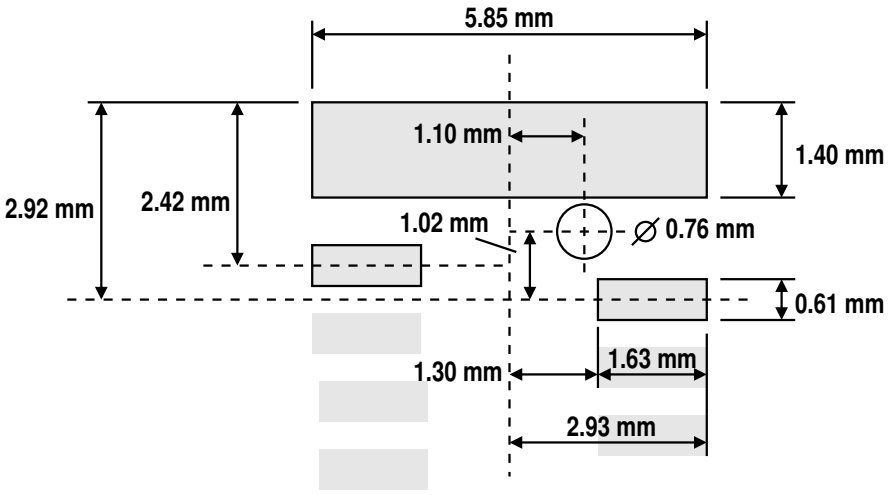
A.5 Common footprint

With the above connectors, we have the choice between the common DF9/M40 design that would need a customization step (i.e., trimming of the positioning pins), and the less common Conan design that could be used without modification.

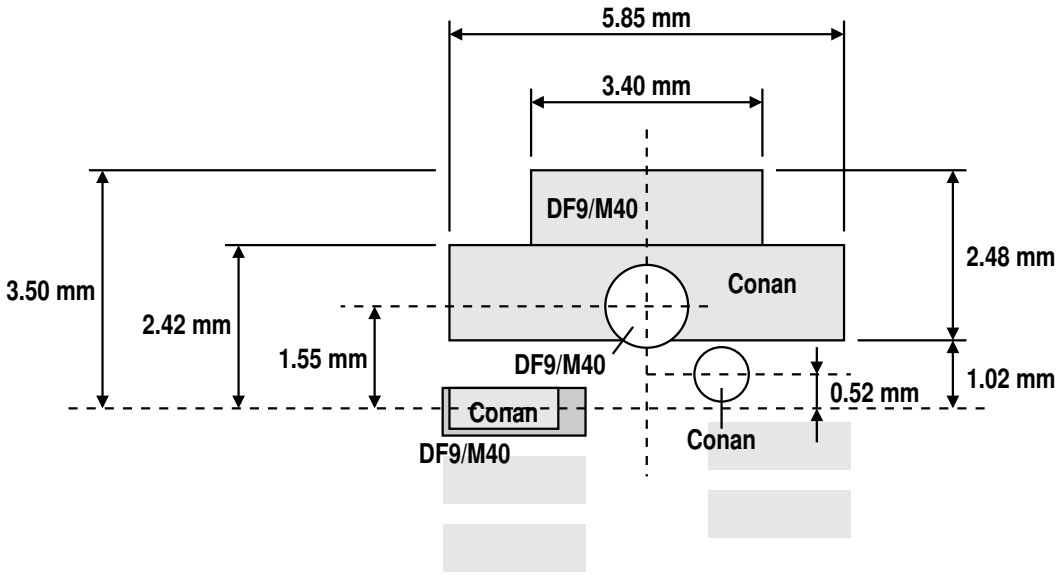
The following drawings illustrate the differences in footprint geometry and the location and size of the positioning pin:



DF9/M40 (above) is generally larger than Conan (below) and places the positioning pins on the center line.



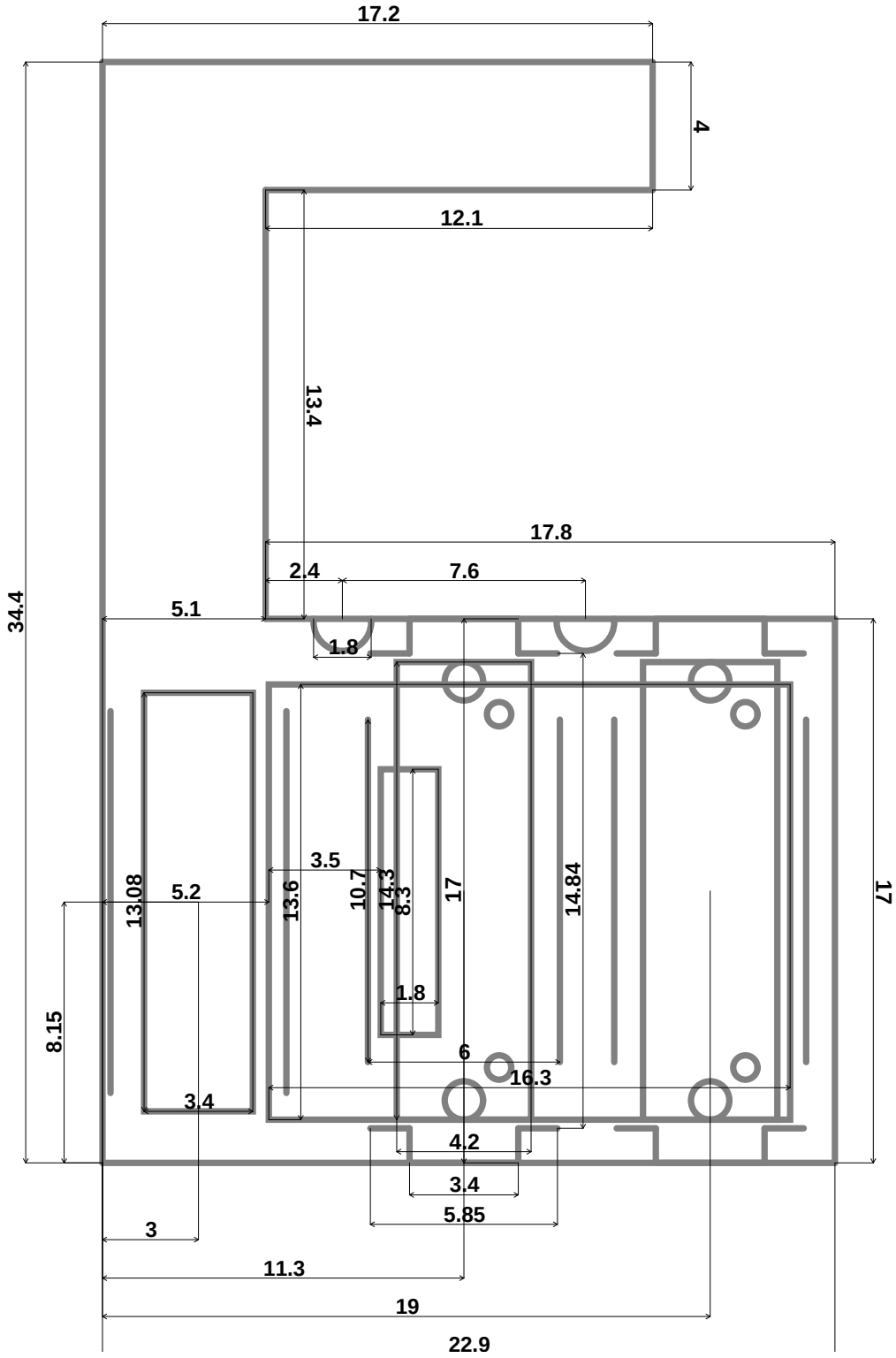
From the above we can derive a common footprint design that should be able to accommodate either type of connector, permitting postponing the component choice until shortly before production and thus reducing sourcing risk:



A.6 Placement overview

The following overview drawing shows the dimensions of BOB, the placement of the Hackerbus main connector (M50), the two board-to-board connectors (DF9/M40), and the memory card.

For each connector, the body is shown as a rectangle and additional lines mark the extent of protruding elements, such as pins or solder tabs. For the memory card, the bounding box and the pad area are shown.



All dimensions are in millimeters.

A.7 Hypothetical pin assignment

To verify that all the required signals can be accommodated in a reasonable way, we provide a hypothetical pin assignment. This assignment is intended as a model reference only and should not constrain the pin assignment choices made for the actual circuit.

As described in section 5, Hackerbus can load VBAT_RAW with up to 1.5 A. Ground return current is the sum of VBAT_RAW, VBUS_OTG (0.5 A), and the signals described in section A.1 (0.5 A), yielding a total of 2.5 A. With each contact being able to carry up to 0.5 A (section A.3), we should therefore provide at least a total of 3 pins for VBAT_RAW and at least 5 pins for ground.

Connector A		Connector B	
FLASH-A	FLASH-K	GND	2V7
VBAT_RAW	VBAT_RAW	CAM-COVER	BATT-LID
VBAT_RAW	USB_HB_DP	I2C-SDA	I2C-SCL
USB_HB_DM	GND	PRIVACY-R	PRIVACY-G
GND	NFC_GND	PRIVACY-B	SD-DAT0
NFC_ANT	GND	SD-DAT1	SD-CLK
GND	VBUS_OTG	SD-CD	SD-VDD
VBAT_SWITCHED	GPIO_d/VDD	SD-CMD	SD-DAT3
UART_TX	UART_RX	SD-DAT2	GPIO_c
UART_CTS	UART_RTS	GPIO_a	GPIO_b
GND		GND	

B References

[1] Reisenweber, Jörg; Almesberger, Werner. *Neo900 Infrared Subsystem*, March 2015. `https://neo900.org/stuff/papers/ir.pdf`

[2] Harwin. *1.27mm pitch DIL SMT vert low-profile socket assy*, M50-315XX42, March 2013. `http://harwin.com/includes/pdfs/M50-315.pdf`

[3] Almesberger, Werner. *Header Part Selection Overview*, January 2016. `http://neo900.org/stuff/papers/hdr.pdf`

[4] Mill-Max Mfg. Corp. *Spring-Loaded Pins – Discrete spring-loaded contacts, through-hole mount*, `https://www.mill-max.com/assets/pdfs/metric/025M.pdf`

[5] NXP Semiconductors. *Level shifting techniques in I^2C-bus design*, AN10441, Rev. 01, June 2007. `http://www.nxp.com/documents/application_note/AN10441.pdf`

[6] Schutte, Herman. *Bi-directional level shifter for I^2C-bus and other systems*, AN97055, August 1997, Philips Semiconductors Systems Laboratory Eindhoven. `http://www.adafruit.com/datasheets/an97055.pdf`